

Claims

What is claimed is:

1. An integrated circuit comprising:
first, second, and third signal terminals;
a chain of series-connected impedance elements with multiple tap points and having endpoints connected to the first and second signal terminals;
a plurality of first switching devices each connected to a respective one of the multiple tap points and to an internal wiper node; and
a configurable output stage connected to the internal wiper node and to the third signal terminal, the configurable output stage comprising a buffer and a second switching device, wherein the second switching device is operable to bypass the buffer.
2. The integrated circuit of claim 1, further comprising a selecting block coupled to control switching of each of the first switching devices, said selecting block comprising a Gray-code counter and a Gray-code decoder.
3. The integrated circuit of claim 2, wherein the switching of a pair of the first switching devices is make-before-break switching.
4. The integrated circuit of claim 1, further comprising a selecting block coupled to control switching of each of the first switching devices, wherein the switching of a pair of the first switching devices is make-before-break switching.

5. The integrated circuit of claim 1, further comprising a memory circuit coupled to store an identity of a single-turned on one of the first switching devices.

6. The integrated circuit of claim 5, wherein the memory circuit is a non-volatile memory circuit.

7. The integrated circuit of claim 1, wherein the configurable output stage further comprises a bias circuit, and the buffer comprises an operational amplifier, and

wherein the bias circuit is controlled to provide a bias to the operational amplifier only when the second switching device is off.

8. The integrated circuit of claim 7, further comprising a memory circuit coupled to store an identity of a single-turned on one of the first switching devices and a status of a configuration signal, said configuration signal controlling the bias circuit and the second switching device.

9. The integrated circuit of claim 1, further comprising a switching circuit that controls switching of the first switching devices, wherein the switching circuit employs Gray code.

10. An integrated circuit, comprising:

first, second, and third signal terminals;

a chain of series-connected impedance elements with multiple tap points and having endpoints connected to the first and second signal terminals;

a plurality of first switching devices each connected to a respective one of the multiple tap points and to an internal wiper node;

a configurable output stage connected to the internal wiper node and to the third signal terminal, the configurable output stage comprising a buffer connected in parallel with a second switching device, wherein a bias circuitry of the buffer and the second switching device are controlled by a configuration signal such that the buffer is biased only when the second switching device is turned-off;

a selecting block indicating an identity of a turned-on one of the first switching devices; and

a memory block for storage of the identity of the turned-on one of the first switching devices, and for the storage of a status of the configuration signal.

11. The integrated circuit of claim 10, wherein the selecting block comprises:

a Gray-code counter; and

a Gray-code decoder, connected after the Gray-code counter to identify the identity of a turned-on one of the first switching devices in accordance with the status of the Gray-code counter.

12. The integrated circuit of claim 11, wherein the selecting block comprises:

a make-before-break circuitry connected between the Gray-code decoder and the first switching devices, the make-before-break circuitry establishing a short overlap conduction time for a pair of the first switching devices, the overlap ensuring that

the internal wiper terminal is always connected to at least one of the tap points.

13. The integrated circuit of claim 10, wherein the selecting block comprises:

a make-before-break circuitry, the make-before-break circuitry establishing a short overlap conduction time for a pair of the first switching devices, the overlap ensuring that the internal wiper terminal is always connected to at least one of the tap points.

14. An integrated circuit comprising:

first and second signal terminals;

a chain of series-connected impedance elements with multiple tap points and having endpoints connected to the first and second signal terminals;

a plurality of first switching devices each connected to a respective one of the multiple tap points and to wiper node; and

a selecting block coupled to control a switching of the first switching devices, the selecting block employing Gray code.

15. The integrated circuit of claim 14, wherein the selecting block comprises:

a Gray-code counter; and

a Gray-code decoder connected after the Gray-code counter to identify a turned-on one of the first switching devices in accordance with the status of the Gray-code counter.

16. The integrated circuit of claim 15, wherein the selecting block further comprises:

a make-before-break circuitry, the make-before-break circuitry establishing a short overlap conduction time for a pair of the first switching devices, the overlap ensuring that the internal wiper terminal is always connected to at least one of the tap points.

17. The integrated circuit of claim 14, wherein the selecting block further comprises:

a make-before-break circuitry, the make-before-break circuitry establishing a short overlap conduction time for a pair of the first switching devices, the overlap ensuring that the internal wiper terminal is always connected to at least one of the tap points.

18. The integrated circuit of claim 14, further comprising a memory circuit coupled to store an identity of a single-turned on one of the first switching devices.

19. The integrated circuit of claim 14, further comprising a configurable output stage connected to the wiper node and to a third signal terminal, the configurable output stage comprising a buffer and a second switching device, wherein the second switching device is operable to bypass the buffer.

20. The integrated circuit of claim 19, further comprising a memory circuit coupled to store an identity of a single-turned on one of the first switching devices and a status of a configuration signal, said configuration signal controlling the second switching device.